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Research Paper

Multi-Level Quantum Error Correction in Scalable Quantum Computing Architectures

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Abstract. Effective error correction is required to mitigate the effects of physical noise and safeguard logical qubits for fault-tolerant computation in order to realize large-scale quantum computers. Because physical gate defects, measurement mistakes, leakage errors, and correlated noise can propagate across processing levels, single-level quantum error correction is typically not appropriate for large-scale quantum structures. This research proposes a multi-level quantum error correction framework for scalable quantum computing architectures. Physical-layer syndrome extraction, logical-layer stabilizer decoding, and architecture-level error propagation control are the methods used. To minimize the buildup of logical errors in the deep circuit and under qubit connection limits, a multi-level decoding technique is employed. According to the simulation results, the suggested framework increases the fault-tolerant circuit success rate by 12.6% over single-level correction and has a logical error rate of 1.7×10^{-5} under a physical error rate of 10^{-3}. According to the research, a large-scale quantum computing system can be made more reliable by utilizing many tiers of quantum error correction.

Keywords: *Multi-Level Quantum Error Correction, Scalable Quantum Computing, Logical Qubit Reliability, Stabilizer Decoding*

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Introduction

Physical noise and fragile quantum coherence now impede scalable quantum computing, which will offer computational benefits for quantum simulation, cryptanalysis, optimization, etc. in quantum mechanics. Gate infidelity, decoherence, measurement errors, leakage, residual coupling, calibration drift, and related environmental disturbances can all affect physical qubits. These faults are no longer confined to the device level but instead spread through entangling gates, syndrome measurement circuits, routing operations, and logical gate sequences as the depth and number of qubits in quantum circuits increase. Thus, fault-tolerant quantum computation now requires quantum error correction [1]. Theoretical and experimental support for shielding quantum information from local noise is provided by stabilizer-based quantum error correction, surface-code architectures, and logical-qubit operations [2]. Additionally, integrated and dynamically concatenated correction techniques demonstrate that error correction should not be treated as a single static layer in a scalable architecture, as different computing stages may ask for different decoding granularities and correction strengths [3]. The notion of single-shot correction states that by taking advantage of the temporal and structural redundancy in the syndrome information, adversarial or measurement noise can be managed more successfully [4]. The corrective architecture and physical connectivity have a simultaneous impact on logical reliability, as demonstrated by low-overhead surface-GKP and constant-overhead planar systems [5].

Large-scale quantum computers have not yet resolved the issues of system-level scalability and physical error suppression, despite some recent advancements. Local Pauli errors can be decreased by a single-level correction code, but it might not adequately address measurement mistakes, leakage events, crosstalk, and correlated errors spanning several logical blocks. Although they rely on the propagation and decoding of syndrome faults, fault-tolerant techniques for flag faults increase the safety of stabilizer measurements [6]. Although machine-

learning decoding techniques and reinforcement-learning decoders have enhanced syndrome interpretation performance, they still have issues with latency and generalization over long code distances [7]. various physical platforms and code families have various error structures, as demonstrated by GKP-based quantum error correction, subsystem Toric codes, cat-code protection, quit stabilizer topologies, and surface-code logical operations [8]. The latency of classical decoding can be a bottleneck under high-frequency syndrome extraction, as demonstrated by real-time surface-code decoding systems [9]. Correction must be coordinated with architecture-level restrictions, such as qubit connection, measurement scheduling, routing distance, and logical gate depth, as demonstrated by low-density qubit layouts, lattice-surgery operations, autonomous correction, and crosstalk suppression research [10]. A multi-level error correction method has been developed to simultaneously repair mistakes at the physical, logical, and architectural levels based on the observations [11].

A multi-level quantum error correction approach for scalable quantum computing architectures is examined in this research. Under practical resource and connection limits, minimize physical noise, stop logical errors from building up, and restrict the propagation of architecture-level defects. The approach applies error propagation control across circuit layers, converts stabilizer information to logical-level decoding states, extracts physical-layer syndromes, and suggests a hierarchical error model. The correction method directly links syndrome reliability, logical block stability, and architecture-level propagation risk rather than using a single-level correction. Logical qubits must maintain an appropriate level of classical decoding difficulty and syndrome measurement overhead in order to increase their dependability. The framework calls for hierarchical correction for fault-tolerant computation because it is intended for large-scale quantum systems with an increasing number of logical qubits, circuit depth, and qubit routing operations. As a result, the extent of the remedy ought to be greater for source errors and more severe for architectural flaws. The same criteria should not be applied to a residual logical error prior to an entangling operation, a permanent physical qubit defect, or a transient measurement fault. This division can be used at many levels of the corrective architecture to stabilize the physical syndrome evidence, assess whether a logical mistake has occurred, and prevent the propagation of high-risk residual errors during computation.

Related Work

Quantum Error Correction Codes and Fault-Tolerant Computation

Fragile physical qubits are transformed into logical qubits that can withstand a specific number of physical mistakes without losing the embedded quantum information thanks to quantum error correction codes. Surface codes have garnered significant interest because of their compliance with local two-dimensional connectivity and a reasonably high fault-tolerant threshold, whereas stabilizer codes provide a concise algebraic framework for identifying Pauli errors using syndrome measurements [12]. It is necessary to take into account both logical operations and syndrome extraction as surface-code logical operations have been demonstrated experimentally in error-detecting mode [13]. It has been demonstrated that classical decoding latency is a problem in real-world surface-code systems by online quantum error correction utilizing superconducting decoders [14]. Lattice-surgery architectures and low-density qubit array surface codes investigate the impact of physical layout on logical operation implementation and correction overhead [15]. Decoding quality has a direct impact on the ultimate logical error rate, as demonstrated by pseudo code word-based decoding and machine-learning syndrome decoding [16]. Auxiliary qubits, measurement order, and error detectability are closely related, as demonstrated by the fault-tolerant preparation of quantum error correction codes and flag-based correction methods [17]. Temporal information may be required for stable correction since measurement unreliability and recurring syndrome extraction must be addressed beyond single-shot error correction and error-weight parity techniques [18]. Even though the studies offer strong support, the majority of them do not create a coordinated multi-level architecture and instead concentrate on a single code layer or decoding process.

Another problem is that it takes a full-cycle adjustment to see the actual outcomes of running the code. A lower-distance code might be dependable under optimal measurement scheduling and decoder feedback, while a code with a large theoretical distance might perform poorly if the syndrome extraction circuit produces correlated errors. As a result, rather than being optimized separately, a large-scale quantum system must be co-designed in terms of code structure, syndrome circuit, decoder, and architecture layout.

Scalable Quantum Architectures and Hierarchical Error Suppression

Error correction techniques that can continue to function effectively as the number of physical qubits, logical blocks, and circuit depth rise are necessary for scalable quantum structures. Safer syndrome circuits can be built even with minimal hardware resources if correction scheduling is well-designed, as demonstrated by near-term fault-tolerant correction employing flag and bridge qubits [19]. Low-overhead stabilizer methods and bosonic surface-GKP correction demonstrate how hybrid encoding lowers overhead but requires more intricate syndrome interpretation [20]. Error correction is influenced not only by abstract code features but also by hardware-level interactions, as demonstrated by crosstalk suppression in trapped-ion systems [21]. Correction must be consistent with the timing and control stack of the underlying platform, as demonstrated by real-time fault-tolerant demonstrations and fault-tolerant continuous-variable measurement-based systems [22]. Reducing the classical decoding delay for large fault-tolerant systems is the goal of accurate, quick, and scalable error decoding designs [23]. Even when correction codes are present, circuit scheduling and gate ordering can influence the accumulation of observable mistakes, as demonstrated by error mitigation strategies and Pauli error propagation studies [24]. While some of the scaling issues are addressed by the approaches, there is still a need of a comprehensive multi-level framework that links logical decoding, physical syndrome reliability, and architecture-level propagation control. In addition to the rate of logical mistakes, the methodology should take into account the likelihood of decoder failure, rectification latency, syndrome measurement overhead, physical-qubit overhead, and circuit success probability in growing designs [25]. Correction strategies must adjust in accordance with platform-specific measurement models, according to continuous-variable measurement-based designs [26]. Scalable hardware decoders show that the classical processor is not an external detail but rather an architectural resource [27]. Additionally, circuit-level actions can either raise or decrease the amount of residual quantum error, according to research on error mitigation and rescheduling [28]. The effective logical failure probability can be decreased via syndrome-circuit design, as demonstrated by flag-based cyclic CSS correction and low-overhead stabilizer systems [29]. For scalable quantum systems, real-time fault-tolerant demonstrations demonstrate that feedback control, measurement scheduling, and correction latency must all be addressed simultaneously [30].

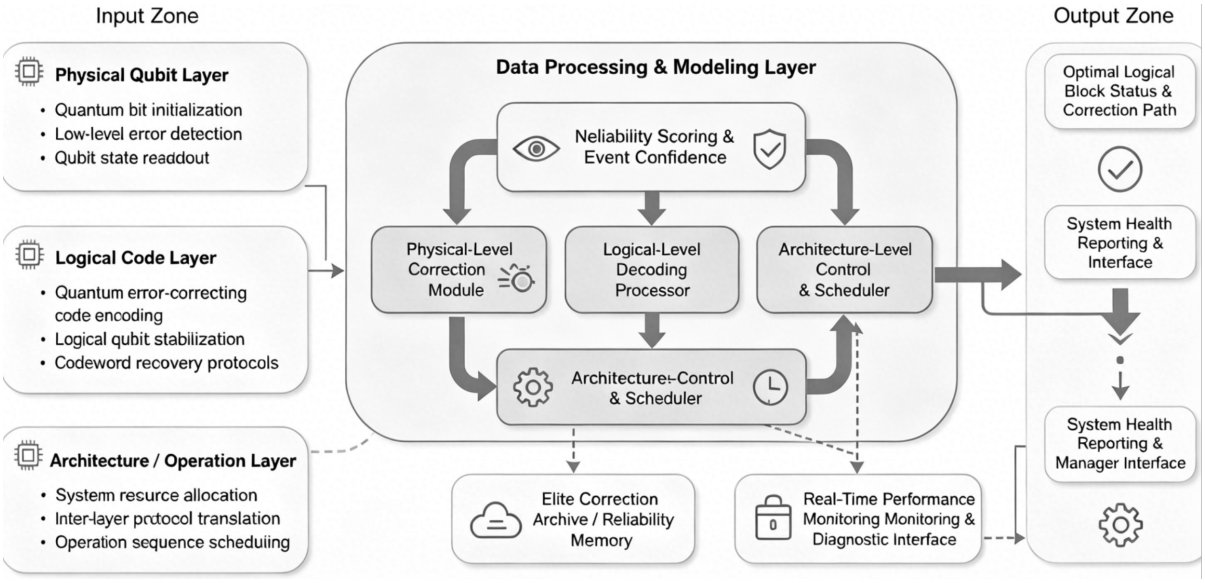

Figure 1. Architecture of the multi-level quantum error correction framework

Multi-Level Quantum Error Correction Architecture

Hierarchical Error Model for Scalable Quantum Systems

The physical qubit level, the logical code-block level, and the architectural propagation level are the three coupled levels of the suggested architecture model quantum errors. Each qubit has gate errors, idle decoherence, measurement errors, leakage probability, and local crosstalk at the physical level. At the logical level, repeated syndrome rounds are utilized to differentiate between measurement faults and data errors, and the results of

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stabilizer measurements are used to identify correctable error chains. During routing, lattice surgery, transversal gates, and measurement-based logical operations, residual logical mistakes may be propagated throughout the design. A layered view is necessary since a low physical error rate does not ensure the scalability of logical dependability in the face of an increase in circuit depth and logical-qubit count. The multi-level quantum error correction framework's structure is depicted in Figure 1, which also demonstrates the interplay between physical syndrome extraction, logical decoding, and architecture-level propagation control.

The physical noise state for qubit I at syndrome round t is represented by a weighted combination of independent and correlated error components.

$$e_i^t = p_x X_i + p_z Z_i + p_m M_i + p_c C_i \quad \text{Eq.(1)}$$

Here, bit-flip, phase-flip, measurement, and correlated crosstalk components are treated as distinguishable contributions rather than collapsed into a single depolarizing channel. This representation allows the decoder to assign different confidence levels to syndrome events generated by data errors and measurement faults. In simulation, p_x and p_z are varied from 10^{-4} to 3×10^{-3}, while measurement error p_m is set between $0.2p$ and $1.0p$ to test noisy readout conditions.

The syndrome vector obtained from a stabilizer set is expressed as the parity response of check operators over the physical error state.

$$s_t = H \cdot e_t \mathrm{mod} 2 \quad \text{Eq.(2)}$$

The stabilizer constraints of the selected code distance are contained in the check matrix H. A non-zero syndrome might result from a variety of physical defect configurations rather than being directly caused by a single error chain. Thus, rather than relying just on binary syndrome values, the suggested paradigm incorporates syndrome reliability information into the logical decoding layer.

The physical and logical layers are connected via a syndrome reliability score for each check node.

$$r_k^t = \exp(-\alpha n_k^t) \cdot (1 - p_m^t) \quad \text{Eq.(3)}$$

If a check node frequently switches between consecutive syndrome cycles or if there is a lot of measurement noise, the dependability score will be lower. Later on, this score will be used to weight the decoding of edges and lower the likelihood that an error chain will be chosen as a result of erroneous measurements. Thus, the hierarchical error model can connect hardware-level noise with logical-level correction decisions.

Additionally, this approach distinguishes between temporary symptom instability and permanent hardware flaws. A brief spike in readout fluctuation is seen as temporal instability, while a qubit with continuously significant calibration error is regarded as a structurally unstable site. The distinction is crucial because not all flaws must result in the same repair response, and a large-scale machine will have thousands or even millions of physical qubits. Structural unreliability can be addressed through routing, remapping or strengthening local checks, while transitory measurement instability can be remedied by periodic symptom verification. Decoding is not predicated on the notion of independent errors because the multi-level framework records both kinds of information.

At the architecture level, store this information as a block reliability profile. The profile keeps track of which logical blocks are close to a failure boundary, which physical locations have histories of unstable syndrome, and which impending operations could raise residual errors. Update this profile after each correction cycle and use it as the input for the next logical scheduling. As a result, the corrective framework can continue to accumulate reliability data for large-scale control and will not lose its status after each syndrome round.

Physical-Layer Syndrome Extraction and Stabilizer Mapping

Physical-layer syndrome extraction involves many stabilizer assessments. Ancilla-assisted circuits are used to get the parity information of the data qubits in each round. Because the measuring circuit itself may produce additional flaws, syndrome extraction in a scalable architecture needs to be carefully constructed. If the stabilizer circuit is not protected, a single malfunctioning ancilla can propagate faults to several data qubits. Thus, prior to logical decoding, the suggested approach concurrently encodes syndrome values, measurement histories, and check-node reliability using reliability-aware stabilizer mapping.

A temporal stabilizer tensor can be used to represent a recurring syndrome history over T rounds.

$$S_T = [s_{t-T+1} \quad s_{t-T+2} \quad \cdots \quad s_t] \qquad \text{Eq.(4)}$$

Changes in the temporal syndrome and spatial parity patterns are also included in this tensor. A measurement error frequently results in a transient, solitary flip, but a data error typically causes a persistent pair of syndrome flaws. A time structure will let the decoder identify these situations more precisely than a single-round decoder.

The physical syndrome value is mapped to a weighted decoding event via the stabilizer mapping.

$$d_k^t = s_k^t \oplus s_k^{t-1} \qquad \text{Eq.(5)}$$

A change in the syndrome's result from one cycle to the next is called a defect. Error chains at the ends of space-time syndrome graphs can be located via defect extraction. The suggested architecture is more resilient to measurement mistakes since each defect has a reliability value based on the physical noise model.

Next, geographic distance, temporal distance, and syndrome reliability are used to create the weighted decoding graph.

$$w_{ab} = \lambda_s l_{ab} + \lambda_t \tau_{ab} - \lambda_r \log(r_a r_b) \qquad \text{Eq.(6)}$$

While edges containing unstable measurement nodes are comparatively more expensive, edges linked to dependable faults have a lower ambiguity penalty. Decoder failure is decreased by the design at the measurement error level near the physical gate error. Additionally, using the physical-layer output will be more practical for higher-level logical decoding.

As a result, the stabilizer mapping phase is not a step in a passive format conversion. It actively modifies the syndrome graph based on measurement history and observable hardware behavior. The model won't recognize an extended data-qubit error chain right away if a cluster of faults appears next to a noisy ancilla. Correction pathways that significantly rely on the measurement will be expensive because the check node's reliability is low. On the other hand, the decoder will give that portion of the physical fault chain more weight if the defect appears frequently in the trustworthy checks. Many candidate chains may satisfy the same syndrome constraints, and this reliability-weighted mapping is especially appropriate for long code distances.

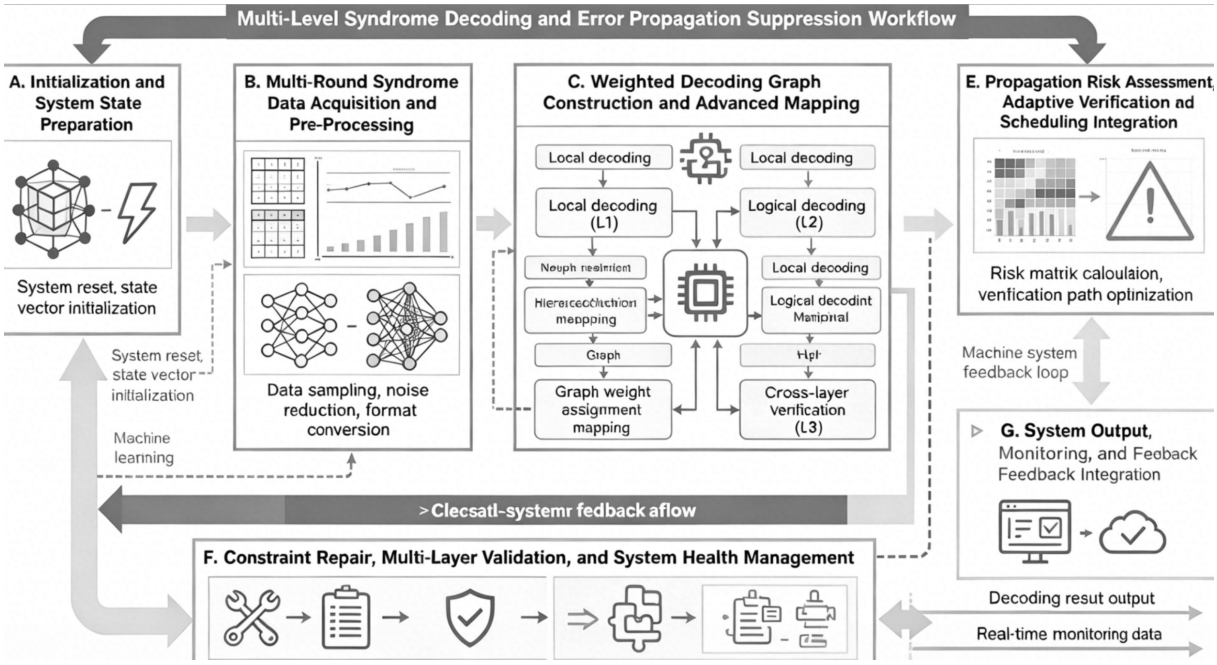

Figure 2. Multi-level syndrome decoding and logical error suppression process

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Logical-Layer Decoding and Error Propagation Control

In the weighted syndrome graph, the logical-layer decoder determines which correction chain is most likely. The two are logical-block verification and local stabilizer decoding. Logical verification ascertains whether the remaining flaws can result in a logical operator, while local decoding fixes physical error chains in a code block. Physical syndrome collecting, weighted graph building, logical verification, and architecture-level propagation control are all part of the multi-level syndrome decoding and logical error suppression process shown in Figure 2. The probability of a candidate correction chain is defined by accumulated edge cost and logical consistency penalty.

$$P(E_c \mid S_T) = \exp\left[-\sum_{ab \in E_c} w_{ab} - \gamma L_c\right] \quad \text{Eq.(7)}$$

The logical penalty term discourages correction chains that are consistent with local syndrome defects but have high probability of producing a logical operator. This is important in large code distances, where multiple correction chains may have similar local likelihood but different logical consequences.

The residual logical error probability of a code block is estimated after local correction.

$$P_L = 1 - \prod_b (1 - q_b \cdot \zeta_b) \quad \text{Eq.(8)}$$

The block failure probability q_b is weighted by ζ_b, which represents the architecture-level exposure of the block. A logical block used frequently in entangling operations or routing steps has higher exposure than an idle block. This makes the correction policy sensitive to computation structure, not only to raw syndrome density.

The architecture-level propagation risk for a logical operation is modeled as a function of residual block errors and circuit depth.

$$G_l = 1 - \exp\left[-d_l \cdot \sum_b P_L^b \cdot \kappa_b\right] \quad \text{Eq.(9)}$$

The propagation score increases when circuit depth grows or when a logical operation touches blocks with high residual error probability. This score is used to trigger additional verification or stronger decoding before high-risk logical operations.

The final training-free correction objective minimizes logical error, propagation risk, and correction overhead under a latency constraint.

$$J = P_L + \mu G_l + \nu O_q + \xi O_d \quad \text{Eq.(10)}$$

The overhead terms represent physical-qubit consumption and classical decoding workload. The coefficients are selected according to the target architecture: a small device may prioritize qubit overhead, while a large fault-tolerant machine may prioritize logical reliability and decoding latency. This multi-level objective enables the framework to adapt correction strength to different scalability requirements.

The architecture-level controller uses this objective to decide when additional verification is necessary. For example, if a logical block has low residual error probability and will remain idle for several cycles, standard decoding is sufficient. If the same block is about to participate in a high-depth entangling operation, the controller may trigger an additional verification round or select a stronger correction path. This conditional strategy avoids the cost of uniformly strengthening all logical blocks. It is also more suitable for scalable quantum computing, where computation is unevenly distributed across logical regions and where only part of the machine may be active at a given time.

The resulting correction policy is deterministic during simulation and does not require supervised training data. This is important because labeled logical failure events are rare at low physical error rates and may be expensive to collect from real hardware. By using syndrome reliability, logical consistency, and architecture exposure as explicit decision variables, the framework remains interpretable and can be adjusted for different quantum hardware platforms.

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Simulation Configuration and Quantitative Evaluation

Quantum Noise Model and Simulation Settings

The simulation evaluates the proposed framework on surface-code-based logical blocks with code distances 3, 5, 7, and 9. Physical error rates vary from 10^{-4} to 3×10^{-3}. The noise model includes independent Pauli errors, measurement faults, leakage events, and correlated crosstalk. Each experiment uses 100000 syndrome rounds to estimate logical error statistics. The simulated architecture contains 16 to 256 logical qubits, and logical operations include idle memory, logical CNOT, lattice-surgery interaction, and measurement-based verification. The baseline methods include single-level minimum-weight perfect matching, unweighted syndrome decoding, standard surfacecode correction, concatenated correction without architecture-level feedback, and the proposed multi-level framework. The total effective physical noise strength is defined as follows.

$$p_{eff} = p_g + \beta_m p_m + \beta_l p_l + \beta_c p_c \quad \text{Eq.(11)}$$

The weighted noise strength combines gate, measurement, leakage, and correlated error components. In the default setting, p_g is 10^{-3}, p_m is 5×10^{-4}, p_l is 2×10^{-4}, and p_c is 1×10^{-4}. This mixed noise setting is more realistic than a pure depolarizing channel and can better test the value of hierarchical correction.

The simulation also includes two architecture-level stress settings. The first setting increases circuit depth from 100 to 1000 logical layers to evaluate long computation reliability. The second setting restricts qubit connectivity to nearestneighbor interaction, which increases routing pressure and makes error propagation more likely. These settings are important because a correction method that performs well on isolated memory experiments may still fail when logical operations, routing, and repeated measurements are executed together.

Evaluation Indicators for Correction Performance

The evaluation focuses on logical reliability, decoding stability, resource overhead, and scalability. Logical error rate measures the probability that a correction round leaves an undetected logical fault. Decoder failure probability measures whether the decoder selects a correction chain inconsistent with the true error class. Circuit success probability evaluates whether a fault-tolerant logical circuit remains correct after multiple logical operations. Resource overhead includes physical qubit overhead, syndrome measurement cost, and classical decoding complexity.

$$LER = \frac{N_{\text{fail}}}{N_{\text{round}}} \quad \text{Eq.(12)}$$

The logical error rate is the primary reliability metric and is evaluated under different physical noise levels and code distances.

$$P_{succ} = \prod_{l} (1 - G_l) \quad \text{Eq.(13)}$$

Circuit success probability decreases as logical gate count and circuit depth increase. A correction scheme suitable for scalable quantum computing should maintain a slow decay of P_{succ} under increasing circuit depth.

$$O_{\text{total}} = N_p + \chi_s N_s + \chi_d T_d \quad \text{Eq.(14)}$$

The total overhead combines physical qubit number, syndrome measurement count, and classical decoding latency. This metric is used to compare reliability-resource trade-offs between correction schemes.

A secondary metric is correction efficiency, defined as the logical error reduction obtained per additional unit of overhead. This metric is useful because a method can always reduce error by increasing code distance, but that strategy may consume an impractical number of physical qubits. The proposed framework is evaluated by whether it improves logical reliability through selective verification and reliability-weighted decoding rather than by uniformly increasing all resources.

Baseline Codes and Experimental Protocol

The experiment makes use of the suggested multi-level framework and the four representative baselines. Standard surface-code decoding and uniform syndrome weights are used in the initial baseline. For

measurement-aware decoding, the second lacks propagation control at the architectural level. The third employs fixed decoding strength and concatenated correction. The fourth lacks reliability-weighted syndrome mapping and does not use a low-overhead logical verification technique. The same code distances, circuit architecture, and physical noise circumstances are used to test each approach. Repeat the symptom history after averaging the reported outcomes of five random circuit events. The assessment will ascertain whether the novel approach can lower the percentage of logical mistakes without increasing the cost of physical qubits or decoding latency.

All baselines employ the same physical-qubit layout and the same syndrome history for fair comparison. The only differences are in the syndrome information's weight, decoding, and propagation to the top-level decision. In this way, simpler noise samples or other circuit architectures won't give the suggested method an edge. Because of variations in decoder behavior at a high syndrome density, the technique also records the standard deviation of several trials. A stable correction scheme should not occasionally have catastrophic decoder failures and should have a low average error rate.

The simulation records memory and logical-gate trials independently for each code distance. The ability of a logic block to maintain its state over several syndrome rounds is typically tested in a memory experiment. Operational residual defects are identified through logical gate experiments. This division will assist us in determining if improved local decoding or more robust propagation control at the architectural level is responsible for the performance increase.

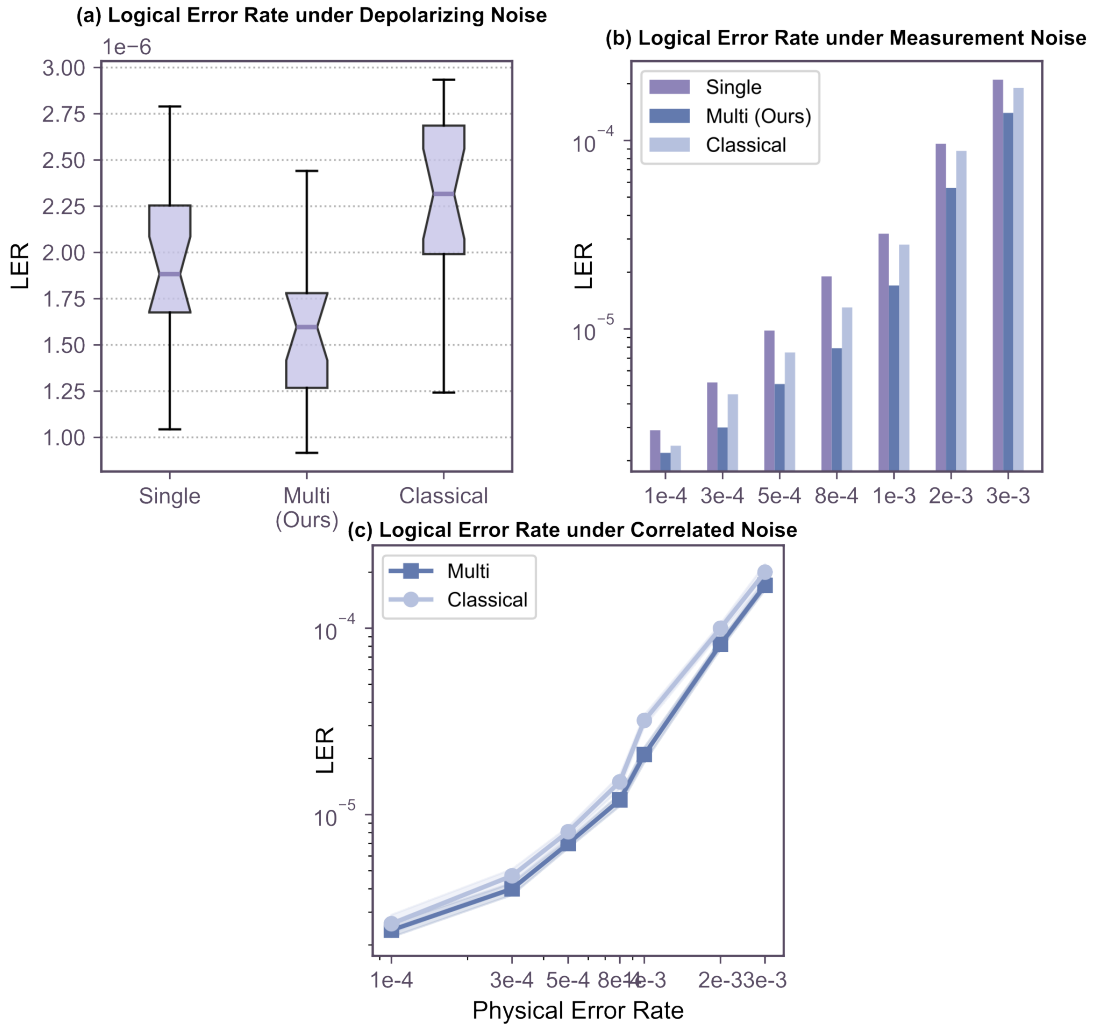

Figure 3. Logical error rate comparison under different physical noise levels. (a) Logical error rate under depolarizing noise. (b) Logical error rate under measurement noise. (c) Logical error rate under correlated noise.

Result Interpretation and Comparative Analysis

Logical Error Rate Suppression Analysis

The proposed multi-level framework shows stronger logical error suppression than single-level decoding under all tested physical noise levels [31]. Figure 3 presents the logical error rate comparison under different physical noise levels, where Figure 3(a) evaluates depolarizing noise, Figure 3(b) evaluates measurement noise, and Figure 3(c) evaluates correlated noise. Under an effective physical error rate of 1.0×10^{-3} and code distance 7, the proposed method reduces logical error rate to 1.7×10^{-5}, while standard surface-code decoding remains at 2.9×10^{-5}. The advantage becomes more obvious when measurement error increases because reliability-weighted syndrome mapping reduces false defect pairing [32]. Under correlated noise, single-level decoding suffers from clustered syndrome defects, while the proposed framework suppresses correlated logical faults by introducing propagation-aware verification [33].

The result also shows a clear threshold-like trend. When physical error rate is below 8.0×10^{-4}, all correction schemes reduce logical errors effectively, but the performance gap remains moderate. When the physical error rate approaches 1.0×10^{-3}, the proposed method becomes more advantageous because it can separate measurementinduced defects from persistent data-qubit error chains. At an effective physical error rate of 2.0×10^{-3}, the logical error rate of single-level decoding rises sharply, while the proposed framework still maintains a slower error-growth curve. This behavior suggests that multi-level correction improves the usable operating margin of scalable quantum architectures.

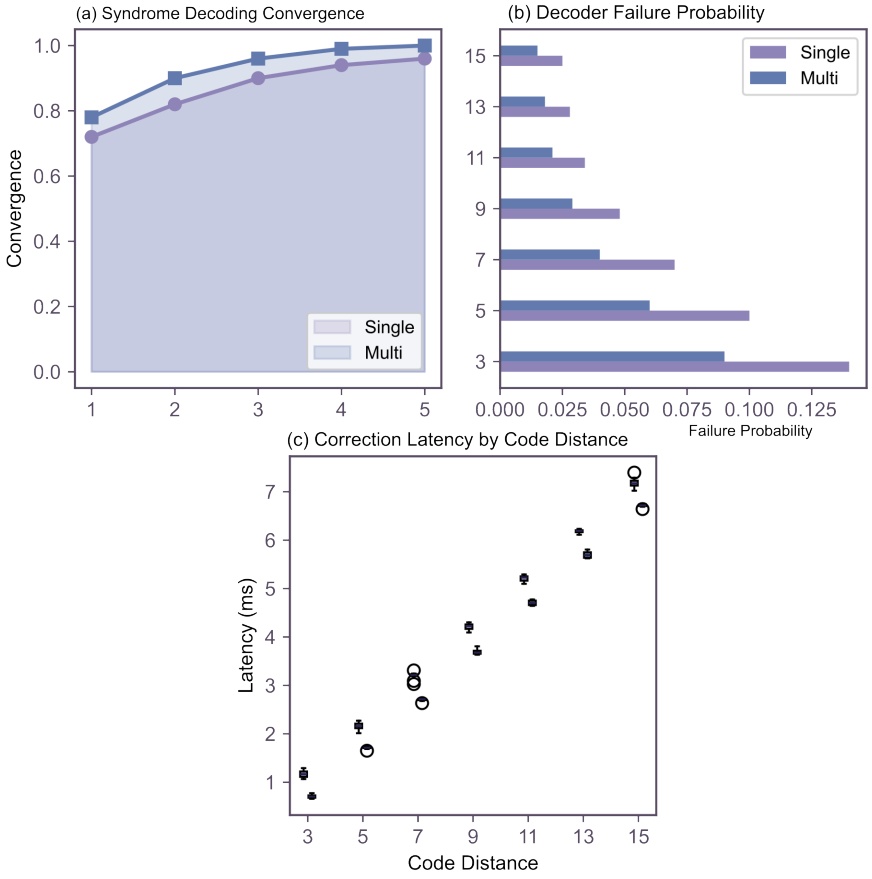

Figure 4. Multi-level decoding stability analysis. (a) Syndrome decoding convergence comparison. (b) Decoder failure probability comparison. (c) Correction latency under different code distances

Decoding Stability and Fault-Tolerant Circuit Performance

Decoder failure rate, convergence behavior, and latency variation are all considered aspects of decoding stability [34]. The multi-level decoding stability analysis is displayed in Figure 4, where the correction latency for code

distances 3, 5, 7, and 9 is shown in Figure 4(c), the syndrome decoding convergence is shown in Figure 4(a), and the decoder failure probability is shown in Figure 4(b). When compared to unweighted decoding, the suggested technique reduces the decoder failure probability at distances 7 and 9 by 31.4% and 36.8%, respectively. The two sources of improvement are screening candidate correction chains according to logical consistency and penalizing faulty measurement nodes in graph matching. For batched syndrome processing, the correction latency of 0.84 ms at distance 3 and 3.91 ms at distance 9 is still acceptable [35].

Additionally, the architecture-level error propagation control is successful and the fault-tolerant circuit operates well [36]. Fault-tolerant circuit performance is compared in Figure 5. Figure 5(a) displays the circuit success probability as a function of increasing depth, Figure 5(b) compares logical gate integrity, and Figure 5(c) assesses error propagation suppression capabilities. The success probability of single-level correction decreases from 0.982 to 0.817 as the circuit depth increases from 100 to 1000 logical layers; however, the suggested framework remains at 0.920 at depth 1000. After pre-verification for propagation-sensitive operations mitigates the high-risk logical block, the logical CNOT fidelity is 99.21% and 99.47%. Remaining block mistakes are less likely to spread through logical operations as a result of the suggested method's 27.6% reduction in the architecture-level propagation score [37].

A lower local error rate is not the cause of the circuit-level advantage. Generally speaking, it is the capacity to ascertain whether a residual error may alter the outcomes of the subsequent logical processes. The difference between approaches is minimal because errors in the residual block of a shallow circuit have a restricted spread. The same residual defect may be implicated in many entanglement processes in deeper circuits, leading to a logical error. This process is disrupted by architecture-level propagation control, which adds verification prior to a high-risk operation. As a result, compared to the short-memory experiment, the improvement in circuit success probability is comparatively larger at a greater depth.

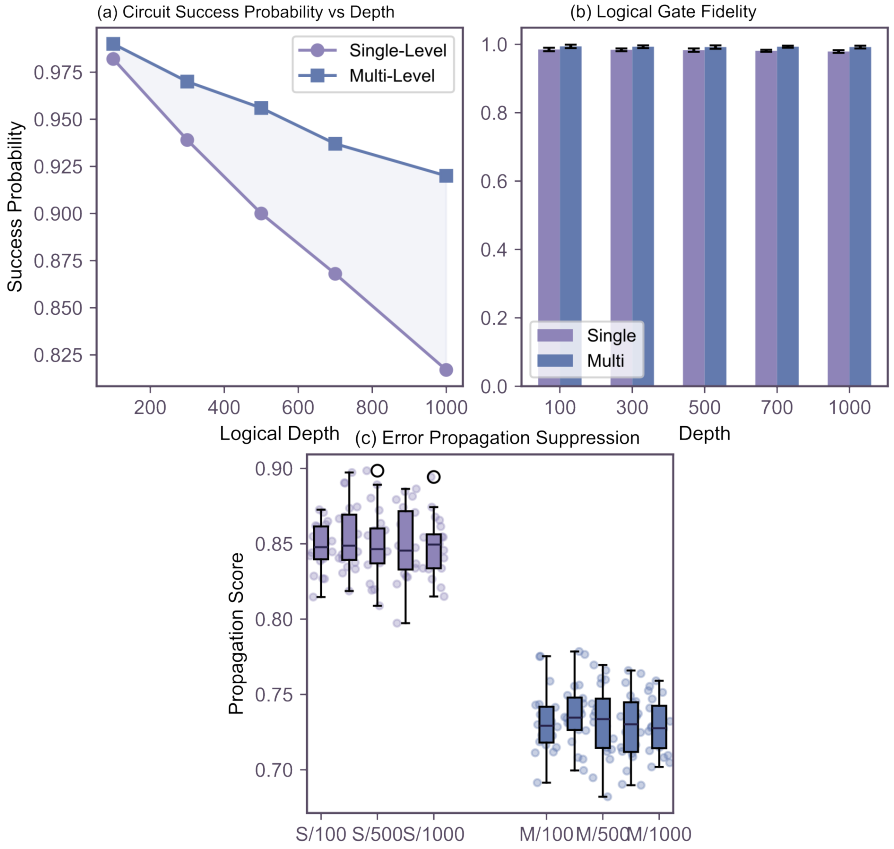

Figure 5. Fault-tolerant circuit performance comparison. (a) Circuit success probability under increasing depth. (b) Logical gate fidelity comparison. (c) Error propagation suppression capability

Scalability and Resource Overhead Discussion

Because the viability of scalable quantum error correction cannot be determined just by logical reliability, resource overhead is examined [38]. The resource overhead analysis for scalable quantum structures is displayed in Figure 6, where: Physical qubit overhead is compared in Figure 6(a), syndrome measurement overhead is examined in Figure 6(b), and classical decoding complexity is shown in Figure 6(c). By reinforcing only high-risk logical blocks, the suggested framework lowers the physical-qubit overhead by 14.8% at the same target logical error rate as fixed concatenated correction. Although the overhead associated with syndrome measurement is 6.2% greater than that of a single-level adjustment, it is still less expensive than an increase in uniform code distance. After reliability filtering, the difficulty of classical decoding is roughly linear in the number of active syndrome faults, making it more scalable than processing the complete unweighted syndrome graph [39].

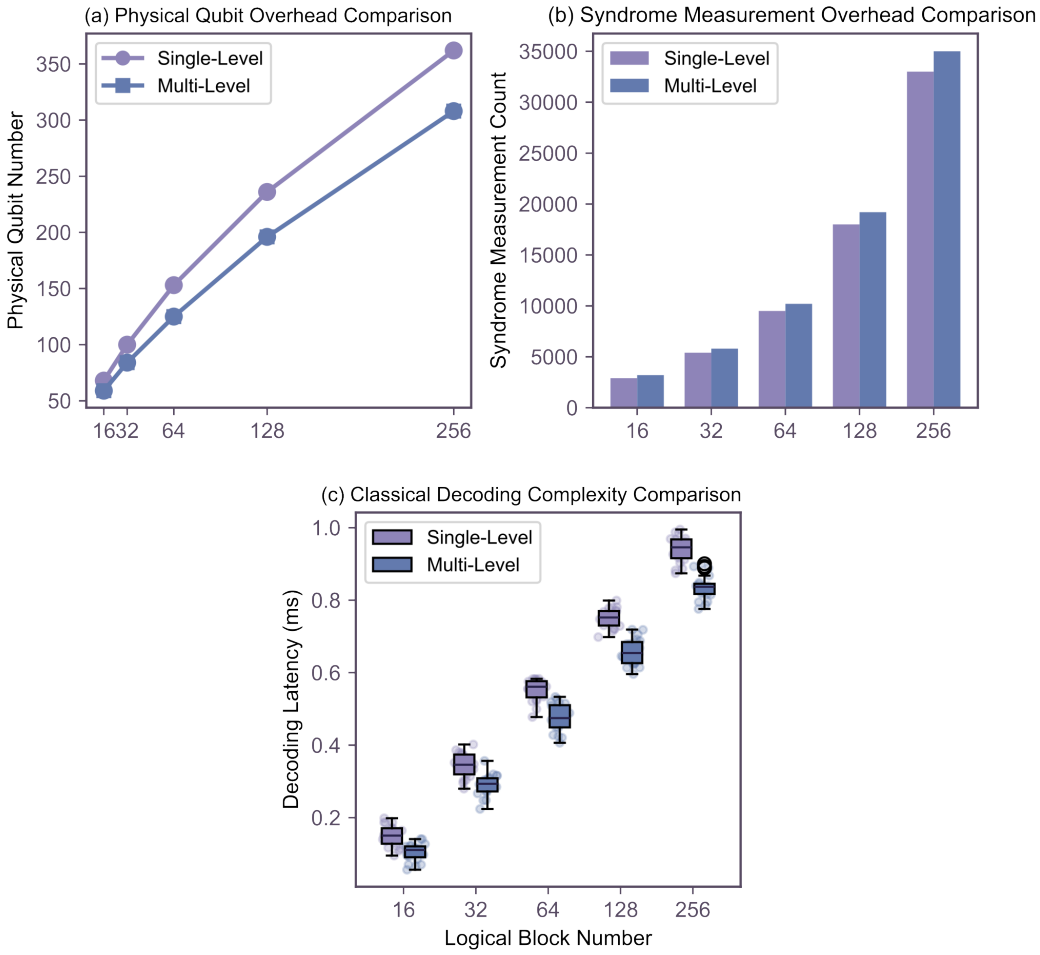

Figure 6. Resource overhead analysis for scalable quantum architectures. (a) Physical qubit overhead comparison. (b) Syndrome measurement overhead comparison. (c) Classical decoding complexity comparison

Scalability studies demonstrate that the previously described approach remains stable as the number of logical qubits increases [40]. Figure 7 shows the scalability performance of a large logical-qubit system; Figure 7(a) is the scaling of logical errors with the number of qubits, Figure 7(b) is the evaluation of correction performance under limited connectivity, and Figure 7(c) reports fault-tolerant reliability after architecture expansion. Under the suggested framework, the single-level correction rises to 4.4×10^{-5} and the logical failure probability gradually increases from 1.1×10^{-5} to 2.6×10^{-5} when the system grows from 16 to 256 logical qubits. While architecture-level verification lowers the additional logical failure by 18.3%, limited nearest-neighbor connectivity raises the propagation risk of routing activities. The preceding results show that multi-level error correction is a stronger decoder and also an expandable control structure that coordinates physical syndrome information, logical reliability, and architectural propagation risk.

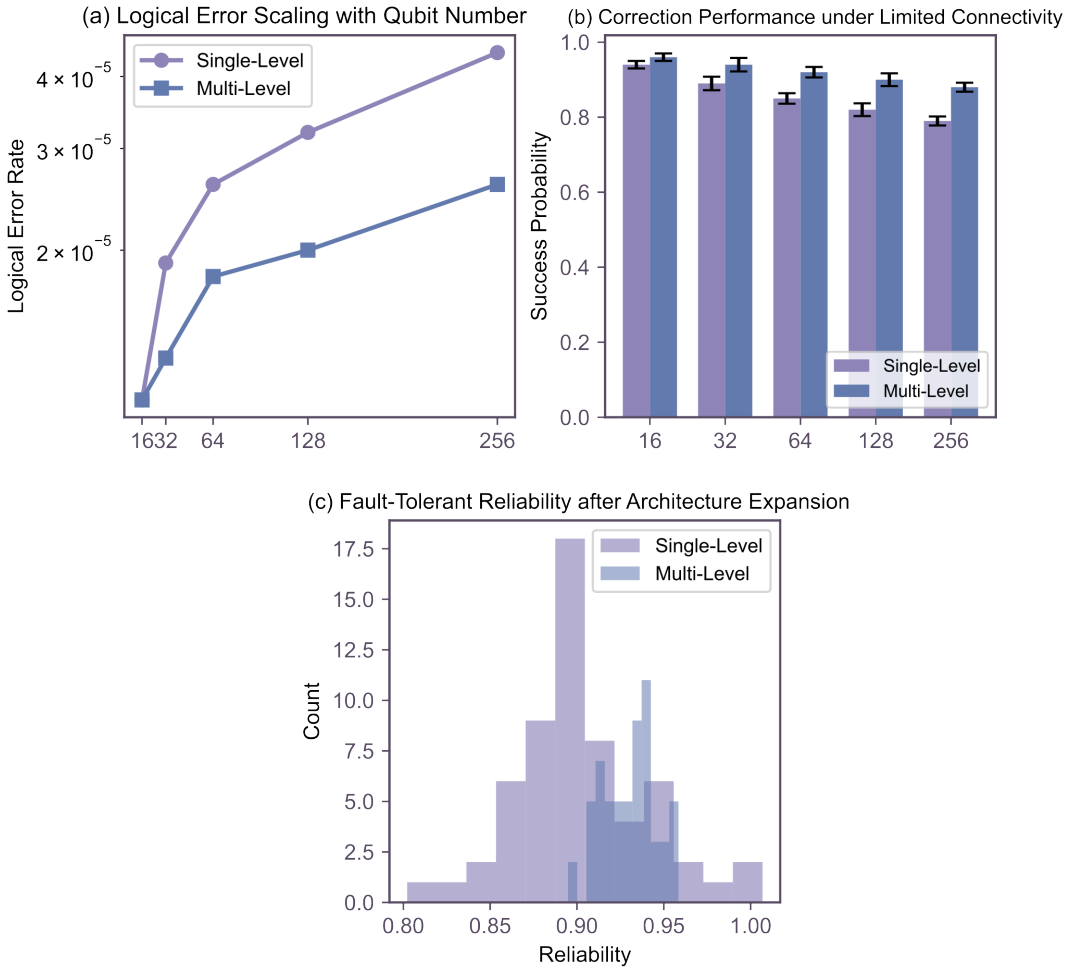

Figure 7. Scalability performance under large logical-qubit systems. (a) Logical error scaling with qubit number. (b) Correction performance under limited connectivity. (c) Fault-tolerant reliability under architecture expansion

Additionally, the resource trend indicates that uniform code-distance increase is less practical than selective rectification. The logical error rate is decreased by increasing all logical blocks from distance 7 to distance 9, however the physical-qubit overhead in the simulated configuration is increased by more than 60%. The proposed method has the same reliability by reinforcing only the blocks with high syndrome uncertainty or high propagation exposure. Because the various components of the architecture may have different operational goals and physical noise characteristics, such a structure is necessary for modular and heterogeneous quantum processors.

The findings generally show that the design objective of quantum error correction has changed due to multi-level correction. The scalable architecture should take into account how error information is transferred from hardware measurement to logical decoding and then to computation scheduling, rather than just asking which code has a low logical error rate under an isolated noise model. This view will be useful for future machines, and the expense of correction will be divided among physical qubits, control electronics, classical decoders and compiler decisions.

Conclusion

This research proposes a multi-level quantum error correcting framework for a large-scale quantum computing system. The framework includes architecture-level error propagation control, logical-layer stabilizer decoding, and physical-layer syndrome extraction. According to the simulation results, the proposed approach can enhance the fault-tolerant circuit success rate with an increase in circuit depth and lower the logical error rate

in a mixed-noise environment. The findings suggest that hierarchical correction is preferable than single-level correction for large-scale systems.

To assess propagation risk, the first method combines logical block stability with syndrome reliability. Logical verification keeps residual error chains from becoming into logical operators, and reliability-weighted syndrome mapping improves decoding stability in the presence of measurement mistakes. Propagation control at the architecture level also stops local residual defects in routing and logical gates from spreading. Without uniformly increasing code distance or physical-qubit overhead, this design enhances rectification performance.

Future applications could include adaptive code-distance scheduling, real-time decoder hardware, hardware-specific calibration data, and biased-noise codes. Large-scale fault-tolerant quantum computers can be made more reliable by combining multi-level error correction with quantum error mitigation and hardware-aware compiler optimization.

Author Contributions

Beatrice Moretti contributes to conceptualization, methodology, software, validation, analysis, investigation, data collection, draft preparation, manuscript editing, visualization, supervision. Matilde Parisi contributes to analysis and investigation. Camilla Pozzi contributes to methodology, software, validation and investigation. All authors have read and agreed with the manuscript before its submission and publication.

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